

MegaMOS™FET

IXTH 20N60 IXTM 20N60

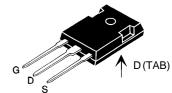
= 600 V= 20 A $R_{DS(on)} = 0.35 \Omega$

N-Channel Enhancement Mode

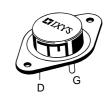


Symbol	Test Conditions			Maximum Ratings	
V _{DSS}	$T_{_{\rm J}} = 25^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$		600	V	
V _{DGR}	$T_J = 25^{\circ}C$ to $150^{\circ}C$; $R_{GS} = 1 M\Omega$		600	V	
V _{GS}	Continuous		±20	V	
\mathbf{V}_{GSM}	Transient		±30	V	
I _{D25}	$T_{c} = 25^{\circ}C$	15N60 20N60	15 20	A A	
I _{DM}	$T_{_{\rm C}} = 25^{\circ}$ C, pulse width limited by $T_{_{\rm JM}}$	15N60 20N60	60 80	A A	
P _D	T _C = 25°C		300	W	
T			-55 + 150	°C	
\mathbf{T}_{JM}			150	°C	
T _{stg}			-55 +150	°C	
\mathbf{M}_{d}	Mountingtorque		1.13/10	Nm/lb.in.	
Weight		TO-204	4 = 18 g, TO-	247 = 6 g	
	Maximum lead temperature for soldering 300 1.6 mm (0.062 in.) from case for 10 s				

TO-247 AD (IXTH)



TO-204 AE (IXTM)



G = Gate,D = Drain, S = Source,TAB = Drain

Features

- International standard packages
- Low R_{DS (on)} HDMOS[™] process
 Rugged polysilicon gate cell structure
- Low package inductance (< 5 nH)
 - easy to drive and to protect
- Fast switching times

Symbol	Test Conditions $(T_J = 25^{\circ}C)$		 ristic Va se speci max.	
V _{DSS}	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	600		V
V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	4.5	V
I _{GSS}	$V_{GS} = \pm 20 V_{DC}, V_{DS} = 0$		±100	nΑ
I _{DSS}	$V_{DS} = 0.8 \bullet V_{DSS}$ $T_{J} = 25^{\circ}C$ $V_{GS} = 0 V$ $T_{J} = 125^{\circ}C$		200 1	μA mA
R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 0.5 I_{D25}$ Pulse test, $t \le 300 \mu\text{s}$, duty cycle $d \le 2 \%$		0.35	Ω

Applications

- Switch-mode and resonant-mode power supplies
- Motor control
- Uninterruptible Power Supplies (UPS)
- · DC choppers

Advantages

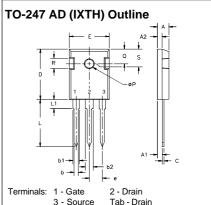
- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- Space savings
- High power density



Symbol	Test Conditions Cha $(T_J = 25^{\circ}\text{C}, \text{ unless c})$ min.	aracter otherwis typ.		
g _{fs}	$V_{DS} = 10 \text{ V}; I_{D} = 0.5 \cdot I_{D25}, \text{ pulse test}$ 11	18		S
C _{iss})	4500		pF
C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	420		pF
\mathbf{C}_{rss}	J	140		pF
t _{d(on)})	20	40	ns
t _r	$V_{GS} = 10 \text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_{D} = 0.5 I_{D25}$	43	60	ns
$\mathbf{t}_{d(off)}$	$R_{\rm G} = 2 \Omega$, (External)	70	90	ns
t _f)	40	60	ns
Q _{g(on)})	150	170	nC
Q_{gs}	$V_{GS} = 10 \text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_{D} = 0.5 I_{D25}$	29	40	nC
\mathbf{Q}_{gd}	J	60	85	nC
R _{thJC}			0.42	K/W
R_{thCK}		0.25		K/W

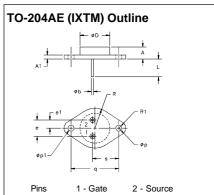
Source-Drain Diode		Characteristic Values			
Symbol Test Conditions		$(T_J = 25^{\circ}C, \text{ unless ot}$ min.			ed)
	V -0V			20	

I _s	V _{GS} = 0 V		20	Α
I _{SM}	Repetitive;		80	Α
V _{SD}	$I_F = I_S$, $V_{GS} = 0$ V, Pulse test, $t \le 300$ μs , duty cycle $d \le 2$ %		1.5	V
t _{rr}	$I_F = I_S$, -di/dt = 100 A/ μ s, $V_R = 100 \text{ V}$	600		ns



Terminals:	1 - Gate	2 - Drain
	3 - Source	Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
Α	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
С	.4	.8	.016	.031
D	20.80	21.46	.819	.845
Е	15.75	16.26	.610	.640
е	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØΡ	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	242	BSC



Case - Drain

Dim.	Millimeter		Inch	nes
	Min.	Max.	Min.	Max.
Α	6.4	11.4	.250	.450
A1	1.53	3.42	.060	.135
Øb	1.45	1.60	.057	.063
ØD		22.22		.875
е	10.67	11.17	.420	.440
e1	5.21	5.71	.205	.225
L	11.18	12.19	.440	.480
Øp	3.84	4.19	.151	.165
Øp1	3.84	4.19	.151	.165
q	30.15	5 BSC	1.187	BSC
R	12.58	13.33	.495	.525
R1	3.33	4.77	.131	.188
S	16.64	17.14	.655	.675

Fig. 1 Output Characteristics

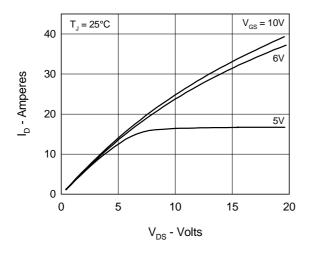


Fig. 3 $R_{DS(on)}$ vs. Drain Current

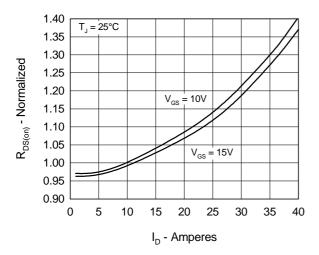


Fig. 5 Drain Current vs.

Case Temperature

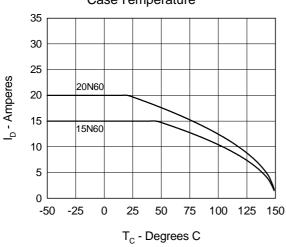


Fig. 2 Input Admittance

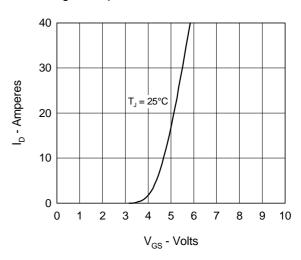


Fig. 4 Temperature Dependence of Drain to Source Resistance

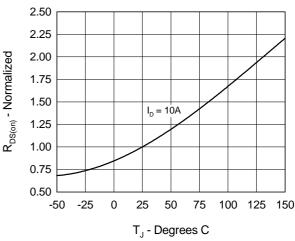


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

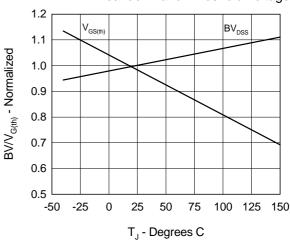




Fig.7 Gate Charge Characteristic Curve

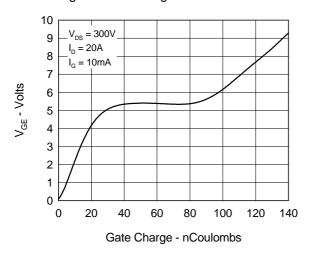
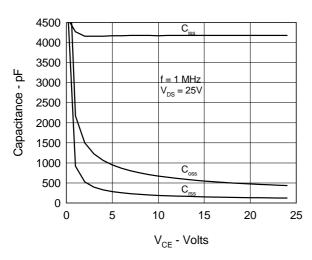


Fig.9 Capacitance Curves



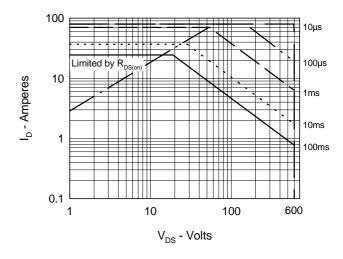


Fig.8 Forward Bias Safe Operating Area

Fig.10 Source Current vs. Source to Drain Voltage

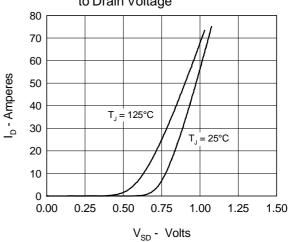


Fig.11 Transient Thermal Impedance

